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EXAMINER

VARTANIAN, HARRY

ART UNIT PAPER NUMBER

2634

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4

Please find below and/or attached an Office communication concerning this application or proceeding.

2

Office Action Summary

Application No.

09/598,870

Applicant(s)

FARLOW, CHARLES S.

Examiner

Harry Vartanian

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 21 June 2000.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-51 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-6, 9-18, 21-33, 35-41 and 43-51 is/are rejected.
- 7) ☒ Claim(s) 7-8, 19-20, 34, 42 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 21 June 2000 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>2.3</u> . | 6) <input type="checkbox"/> Other: _____ |

Detailed Action

Information Disclosure Statement

1. The information disclosure statement filed June 21, 2000(Paper #2) fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each U.S. and foreign patent; each publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the information referred to therein has not been considered. Certain book listings were not readily found. Please provide in the future if you would like consideration of that prior art. Documents that were found online and in IEEE were added to file wrapper and considered.

Claim Objections

1. Claim 16 and 26 recites the limitation "the feedback signal". There is insufficient antecedent basis for this limitation in the claim or in Claim 15 and 25, respectively. It is recommended that both Claims be changed to include "decoder bank provides a feedback signal..."

2. Claim 37 and 40-42 recites the limitation "the parallel outputs" of the bank of adaptive equalizers. There is insufficient antecedent basis for this limitation in the claim. It is suggested that line 13 of Claim 37 be changed to "equalizing the signal in parallel in a bank of adaptive equalizers **with parallel outputs**".

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Drawings

3. The drawings are objected to under 37 CFR 1.83(a) because they fail to show a **control signal 314 in fig 3** as described in the specification **on page 8 line 12**. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

4. The drawings are objected to under 37 CFR 1.83(a) because they fail to show a **decoder bank 412 in fig 4** as described in the specification **on page 10 line 19**. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claim 27 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the

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claimed invention. In Claim 27 it is stated that the circuits process CRCs for Ethernet packets. Examiner found no such limitation or disclosure in the specifications.

Claim Rejections - 35 USC § 102

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

6. Claim 28-31 is rejected under 35 U.S.C. 102(e) as being unpatentable over Rakib et al (US Patent# 6665308). Regarding Claim 28, Rakib et al meets the following limitations:

a time division multiple access (**Column 8, Lines 10-50; fig 57**) communication channel, the method comprising:

receiving a signal over the communication channel; **fig 1**

equalizing the signal in a plurality of equalizers; (**Column 90, Lines 43-53**)

and selecting an output of one of the equalizers. **Claim 12**

Regarding Claim 29, Rakib et al meets the following limitations:

wherein receiving a signal over the communication channel comprises receiving the signal over a wireless communication channel. (**Column 51, Lines 45-53**)

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Regarding Claim 30, Rakib et al meets the following limitations:

wherein receiving a signal over the communication channel comprises receiving the signal over a communication channel of a hybrid fibercoax network. **(Column 13, Lines 66-67)**

Regarding Claim 31, Rakib et al meets the following limitations:

wherein equalizing the signal comprises equalizing the signal in a bank of equalizers. **(Column 90, Lines 43-53)**

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
 2. Ascertaining the differences between the prior art and the claims at issue.
 3. Resolving the level of ordinary skill in the pertinent art.
 4. Considering objective evidence present in the application indicating obviousness or nonobviousness.
7. Claim 1-2 and 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Peile(US Patent# 4,821,289) in view of Gollamudi (see 892). Regarding Claim 1, Peile meets the following limitations:

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an input adapted to receive signals from a communications channel; a plurality of equalizer circuits coupled to the input and operable to generate a plurality of intermediate signals;

Claim 1

an output coupled to the selector circuit that receives the selected intermediate signal. **Claim 6**

Peile fails to teach the use of a selector circuit for choosing one of the output signals from the plurality of equalizers.

However, Gollamudi discloses the use of such a selector circuit in figure 2 of his adaptive parallel equalization system. Therefor it would have been prima facie obvious to those skilled in the art at the time of the invention to use a switch or selector circuit to chose one of the outputs from a bank of parallel equalizers. The motivation to combine is that it is well known in the art that in a parallel configuration of equalizers, memory elements, channels etc. a switch is commonly used to selectively choose one of the plurality of connections or paths based on which equalizer has the best estimate of the channel(e.g. Rake receiver for CDMA).

Regarding Claim 2, Peile meets the following limitations:

wherein each of the plurality of equalizer circuits comprises one of a fixed equalizer and an adaptive equalizer. **(Column 2, lines 29-38)**

Regarding Claim 4, Peile meets the following limitations:

wherein each of the adaptive equalizers comprises one of a transversal structure and a lattice structure. **Abstract**

Regarding Claim 5, Peile meets the following limitations:

wherein each of the adaptive equalizers uses one of a recursive least squares adaptation algorithm, a least mean-square adaptation algorithm, a zero forcing adaptation algorithm, a gradient recursive least squares adaptation algorithm, a fast recursive least squares adaptation algorithm and a square root recursive least squares adaptation algorithm. **(Column 1, Lines 38-50)**

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Regarding Claim 6, Peile meets the following limitations:

wherein the plurality of equalizer circuits provides a signal that reflects the relative quality of the intermediate signals from the plurality of equalizer circuits to the selector circuit to select the intermediate signal. **(Column 2, Lines 20-52)**

8. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Peile(US Patent# 4,821,289) in view of Gollamudi (see PTO-892) further in view of Suzuki (US Patent# 5,602,507). Peile and Gollamudi meet all the limitations of Claim 3(see above paragraphs) except for specifying that the adaptive equalizer is linear or nonlinear.

However, Suzuki discloses that:

"adaptive equalizers have been used as the adaptive receivers. From the view point of the arrangements of the adaptive equalizers, the adaptive equalizers can be classified into linear equalizers and non-linear equalizers."
(Column 1, Lines 30-34)

Therefor it would have been prima facie obvious to one having ordinary skill in the art at the time the invention was made to have an adaptive equalizer be linear or nonlinear. The motivation to combine is that the use of a linear equalizer can be easily implemented in hardware. Moreover, the use of non-linear equalizers can result in more accurate filter coefficient calculations in high multi-path environments.

9. Claim 9, 11, and 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Peile(US Patent# 4,821,289) in view of Gollamudi (see 892). Regarding Claim 9, Peile meets the following limitations:

an input adapted to receive signals from a communication channel; **fig 2**

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an equalizer bank having at least two equalizers coupled in parallel and coupled to the input; **Claim 1, fig 2**

a decoder bank having at least two error correction decoder circuits coupled in parallel, each error correction decoder circuit coupled to a corresponding one of the at least two equalizers of the equalizer bank; **See Abstract and fig 2**

Peile fails to teach the use of a selector circuit for choosing one of the output signals from the plurality of equalizers.

However, Gollamudi discloses the use of such a coupled selector circuit in figure 2 of his adaptive parallel equalization system. Therefor it would have been prima facie obvious to those skilled in the art at the time of the invention to use a switch or selector circuit to chose one of the outputs from a bank of parallel equalizers. The motivation to combine is that it is well known in the art that in a parallel configuration of equalizers, memory elements, channels etc. a switch is commonly used to selectively choose one of the plurality of connections or path based on which equalizer has the best estimate of the channel(e.g. Rake receiver for CDMA).

Regarding Claim 11, Peile meets the following limitations:

wherein each of the at least two equalizers comprises one of a fixed equalizer and an adaptive equalizer. **(Column 2, Lines 29-38)**

Regarding Claim 13, Peile meets the following limitations:

wherein each of the adaptive equalizers comprises one of a transversal structure and a lattice structure. **Abstract**

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Regarding Claim 14, Peile meets the following limitations:

wherein each of the adaptive equalizers uses one of a recursive least squares adaptation algorithm, a least mean-square adaptation algorithm, a zero forcing adaptation algorithm, a gradient recursive least squares adaptation algorithm, a fast recursive least squares adaptation algorithm and a square root recursive least squares adaptation algorithm. **(Column 1, Lines 38-50)**

Regarding Claim 15, Peile meets the following limitations:

wherein the decoder bank provides feedback to the at least two equalizers of the equalizer bank.
(Column 2, Lines 20-52)

Regarding Claim 16, Peile meets the following limitations:

wherein the feedback signal is also provided to the selector circuit to be used in selecting the output of one of the at least two equalizer circuits. **(Column 2, Lines 20-52)**

10. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Peile(US Patent# 4,821,289) in view of Gollamudi (see PTO-892) further in view of Schilling (US Patent# 6,466,610). Peile and Gollamudi meet all the limitations of Claim 10(see above paragraphs) except for disclosing the use of FEC in their decoders.

However, Schilling discloses that:

"The receiver has a multiplicity of receiver subsystems which include a plurality of receiver antennas. Each subsystem corresponding to a receiver antenna has a plurality of matched filters. As shown in FIG. 6, by way of example, a first receiver antenna RA1 and a second receiver antenna RA2 are shown. The first receiver antenna RA1 is coupled to a first matched filter 24 and a second matched filter 34. The second receiver antenna RA2 is coupled to a fifth matched filter 25 and a sixth matched filter 35. The RAKE and space-diversity combiner 60 combines the outputs from the first matched filter 24, the second matched filter 34, the fifth matched filter 25, and the sixth matched filter 35 to form a combined signal. The de-interleaver 61 de-interleaves the combined signal, and the FEC decoder 62 decodes the de-interleaved signal." **(Column 12, line 64 to Column 13, Line 11)**

Therefor it would have been prima facie obvious to one having ordinary skill in the art at the time the invention was made to use forward error correction (FEC) in a decoder. The

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motivation to use FEC is that it can reduce bit errors and the bit error rate of the communication system.

11. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Peile(US Patent# 4,821,289) in view of Gollamudi (see PTO-892) further in view of Suzuki (US Patent# 5,602,507). Peile and Gollamudi meet all the limitations of Claim 12(see above paragraphs) except for specifying that the adaptive equalizer is linear or nonlinear.

However, Suzuki discloses that:

"adaptive equalizers have been used as the adaptive receivers. From the view point of the arrangements of the adaptive equalizers, the adaptive equalizers can be classified into linear equalizers and non-linear equalizers." **(Column 1, Lines 30-34)**

Therefor it would have been prima facie obvious to one having ordinary skill in the art at the time the invention was made to have an adaptive equalizer be linear or nonlinear. The motivation to combine is that the use of a linear equalizer can be easily implemented in hardware. Moreover, the use of non-linear equalizers can result in more accurate filter coefficient calculations in high multi-path environments.

12. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Peile(US Patent# 4,821,289) in view of Gollamudi (see PTO-892) further in view of Kurtz (US Patent #6,574,207). Peile and Gollamudi meet all the limitations of Claim 17(see above paragraphs) except the use of buffers in a decoder.

However, Kurtz discloses that:

"FIG. 8A is a block diagram of the Ultra High Speed Data Decoder of the present invention. The data expansion process is the inverse of the data compression process, and the Decoder includes an optional Transmission Decoding process 801, a Gain Decoder 810, a Data Sample Dequantizer 820, an optional Sample Format Re-Processor 830, and an optional Buffer 840. The optional

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Transmission Decoding process 801 includes a Deinterleaver 803 and a FEC Decoder 802.”
(Column 15, Lines 29-38)

Therefor it would have been prima facie obvious to one having ordinary skill in the art at the time the invention was made to have buffers in a decoder. The motivation to combine is that buffers are sometimes needed to temporarily store information during the process of decoding.

13. Claims 18, 21, and 23-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Peile(US Patent# 4,821,289) in view of Gollamudi (see PTO-892). Regarding Claim 18, Peile meets the following limitations:

an input adapted to receive signals from a communication channel; **fig 2**

an equalizer bank having at least two equalizers coupled in parallel and coupled to the input;
Claim 1, fig 2

a first decoder bank having at least two packet decoder circuits coupled in parallel, each packet decoder circuit responsive to a corresponding one of the at least two equalizers of the equalizer bank; **Abstract ,fig 2**

Peile fails to teach the use of a selector circuit for choosing one of the output signals from the plurality of equalizers.

However, Gollamudi discloses the use of such a coupled selector circuit in figure 2 of his adaptive parallel equalization system. Therefor it would have been prima facie obvious to those skilled in the art at the time of the invention to use a switch or selector circuit to chose of the outputs from a bank of parallel equalizers. The motivation to combine is that it is well known in the art that in a parallel configuration of equalizers, memory elements, channels etc. a switch is commonly used to selectively choose one of the plurality of connections or paths based on which equalizer has the best estimate of the channel(e.g. Rake receiver for CDMA).

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Regarding Claim 21, Peile meets the following limitations:

wherein each of the at least two equalizers comprises one of a fixed equalizer and an adaptive equalizer. **(Column 2, lines 29-38)**

Regarding Claim 23, Peile meets the following limitations:

wherein each of the adaptive equalizers comprises one of a transversal structure and a lattice structure. **Abstract**

Regarding Claim 24, Peile meets the following limitations:

wherein each of the adaptive equalizers uses one of a recursive least squares adaptation algorithm, a least mean-square adaptation algorithm, a zero forcing adaptation algorithm, a gradient recursive least squares adaptation algorithm, a fast recursive least squares adaptation algorithm and a square root recursive least squares adaptation algorithm. **(Column 1, Lines 38-50)**

Regarding Claim 25, Peile meets the following limitations:

wherein the first decoder bank provides feedback to the at least two equalizers of the equalizer bank. **(Column 2, Lines 20-52)**

Regarding Claim 26, Peile meets the following limitations:

wherein the feedback signal is also provided to the selector circuit to be used in selecting the output of one of the at least two equalizer circuits. **(Column 2, Lines 20-52)**

14. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Peile(US Patent# 4,821,289) in view of Gollamudi (see PTO-892) further in view of Suzuki (US Patent# 5,602,507). Peile and Gollamudi meet all the limitations of Claim 22(see above paragraphs) except for specifying that the adaptive equalizer is linear or nonlinear.

However, Suzuki discloses that:

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"adaptive equalizers have been used as the adaptive receivers. From the view point of the arrangements of the adaptive equalizers, the adaptive equalizers can be classified into linear equalizers and non-linear equalizers." **(Column 1, Lines 30-34)**

Therefor it would have been prima facie obvious to one having ordinary skill in the art at the time the invention was made to have an adaptive equalizer be linear or nonlinear. The motivation to combine is that the use of a linear equalizer can be easily implemented in hardware. Moreover, the use of non-linear equalizers can result in more accurate filter coefficient calculations in high multi-path environments.

15. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Peile(US Patent# 4,821,289) in view of Gollamudi (see PTO-892) further in view of Szczepanek (US Patent #5,299,193). Peile and Gollamudi meet all the limitations of Claim 27(see above paragraphs) except for specifying the use of CRC on Ethernet packets.

However, Szczepanek discloses that:

The third output of delimiter decoder 54 is connected to one of the five inputs of a data insertion multiplexer 68. Multiplexer 68 also receives at two of its inputs the STSM (serial transmit state machine) and MSM (monitor state machine) signals respectively. A fourth input to multiplexer 68 is the output of a serial receive state machine 70. The final input of multiplexer 68 is connected to receive the TX.sub.-- DATA signal. The TX.sub.-- DATA signal is received from circuitry discussed below in connection with FIG. 4c. Additionally, multiplexer 68 provides an output signal INSERT.sub.-- DATA which is provided to circuitry discussed below in connection with FIG. 4b. Serial or receive state machine 70 also receives input signals from baud sample latches block 56, CRC checker 60 and flag logic block 62. A receive slot timer 72 is also associated with serial receive state machine 70 for serving the function of ensuring ethernet received frames are at least 64 bytes long. **(Column 11, Lines 15-32)**

Therefor it would have been prima facie obvious to one having ordinary skill in the art at the time the invention was made to use CRC on Ethernet packets in a decoder. The motivation to combine is that CRC is commonly used for error detection in communication systems.

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16. Claim 32 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rakib et al (US Patent# 6665308) in view of Peile (US Patent #4821288). Rakib et al meets all the limitations of Claim 32(see above paragraphs) except for the disclosing the "loading selected coefficients...prior to receiving the signal."

However, Peile discloses that:

"A significant feature of the invention is that equalization (using a Kalman filter, for example) is performed on the data in each of the time windows A-G of FIG. 4b using separate equalizers for each of the windows. Thus, each time window has its own set of multiplier coefficients (stored in a corresponding one of the tap registers 144a-g and 146a-g) and its own tap update processor (156a-g). Each tap update processor controls the contents of the corresponding pair of tap registers (i.e., the multiplier coefficients) for its own time window independently of all other tap update processors and tap registers. Of course, as illustrated in FIG. 4b, there is some overlap in the data contained in each time window, so that there may be some coincidental correlation between the equalization processes performed in adjacent ones of the time windows A-G of FIG. 4b depending upon codeword length and number of codewords in each interleaved block..."
(Column 10, Lines 18-60)

Therefor it would have been prima facie obvious to one having ordinary skill in the art at the time the invention was made to load the filter coefficients prior to reception. The motivation to combine is that loading the coefficient right before processing the new received signals can help to ensure that the filter coefficients have the most up to date information about the channel conditions

17. Claim 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rakib et al (US Patent# 6665308) in view of Kurtz (US Patent #6,574,207). Rakib et al meets all the limitations of Claim 33(see above paragraphs) except the use of buffers in his receiver.

However, Kurtz discloses that:

"FIG. 8A is a block diagram of the Ultra High Speed Data Decoder of the present invention. The data expansion process is the inverse of the data compression process, and the Decoder includes an optional Transmission Decoding process 801, a Gain Decoder 810, a Data Sample Dequantizer 820, an optional Sample Format Re-Processor 830, and an optional Buffer 840. The optional Transmission Decoding process 801 includes a Deinterleaver 803 and a FEC Decoder 802."
(Column 15, Lines 29-38)

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Therefor it would have been prima facie obvious to one having ordinary skill in the art at the time the invention was made to have buffers in a decoder. The motivation to combine is that buffers are sometimes needed to temporarily store information during the process of decoding.

18. Claims 35 -36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rakib et al (US Patent# 6665308) in view of Peile(US Patent# 4,821,289). Regarding Claims 35-36, Rakib et al meets all the limitations(see above paragraphs) except for the use of a quality measure of the output of the equalizers(Claim 35) with that measure being the one of the mean-squared error and a peak error.

However, Peile meets the following limitations of Claims 35 and 36:

further comprising generating a quality measure of the output of each of the plurality of equalizers. **(Column 1, Lines 38-50)**

wherein generating a quality measure comprises generating one of a mean-squared error and a peak error over a selected interval. **(Column 1, Lines 38-50)**

Therefor it would have been prima facie obvious to one having ordinary skill in the art at the time the invention was made to generate a quality of an equalizer by using mean-squared error or a peak error. The motivation to combine is that adaptive equalizers typical use some form of error measurement, such as mean-squared, in order to determine the quality of the filter coefficients of the equalizer.

19. Claims 37 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Peile(US Patent# 4,821,289) in view of Kurtz (US Patent #6,574,207) further in view of Gollamudi(see PTO-892). Regarding Claim 37, Peile meets the following limitation:

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receiving a signal over the communication channel; **fig 2**
equalizing the signal in parallel in a bank of adaptive equalizers; **(Claims 1 and 2)**
further processing the parallel outputs of the bank of adaptive equalizers; **(Claims 1 and 2)**
generating a quality measure of the output of each of the bank of adaptive equalizers;
(Column 1, Lines 38-50)

Peile fails to disclose the use of his system for TDMA, the use of buffers, and the use of a selector circuit.

However, Kurtz meets the following limitations:

a time division multiple access communication channel **(Column 6, line 62 to column 7 line 43)**

buffering the parallel outputs of the bank of adaptive equalizers; **(Column 15, Lines 29-38)**

Therefor it would have been prima facie obvious to one having ordinary skill in the art at the time the invention was made use Peile equalizer system for TDMA with output buffers. The motivation to combine is that wireless TDMA systems, like GSM, suffer from a constantly changing channel due to multipath fading. Therefor the use of multiple adaptive equalizers can help in reduce the effects of fading. Regarding the use of buffers, buffers are sometimes needed to temporarily store information during the process of decoding.

Moreover, Gollamudi meets the following limitation:

selecting an output of one of the equalizers based on the quality measure **fig 2**

Therefor it would have been prima facie obvious to those skilled in the art at the time of the invention to use a switch or selector circuit to chose of the outputs from the bank of parallel equalizers disclosed by Peile and Kurtz's invention. The motivation to combine is that it is well known in the art that in a parallel configuration of equalizers, memory elements, channels etc. a switch is commonly used to selectively choose one of the plurality

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of connections or path outputs based on which equalizer has the best estimate of the channel.

Regarding Claim 38, Kurtz meets the following limitation:

wherein receiving a signal over the communication channel comprises receiving the signal over a wireless communication channel. **fig 1**

20. Claims 39 is rejected under 35 U.S.C. 103(a) as being unpatentable over Peile(US Patent# 4,821,289) in view of Kurtz (US Patent #6,574,207) further in view of Gollamudi(see PTO-892) further in view of Rakib et al(US Patent# 6665308). Regarding Claim 39, Peile, Kurtz, and Gollamudi meet all the limitations of the Claim(please see above paragraphs) except for the use of the equalizing method in a hybrid fiber coax system.

However, Rakib et al meets the following limitations in his equalizer:

wherein receiving a signal over the communication channel comprises receiving the signal over a communication channel of a hybrid fiber-coax network. **(Column 13, Lines 66-67)**

Therefor it would have been prima facie obvious to those skilled in the art at the time of the invention to use the equalizing method disclosed in Claim 37 on a hybrid fiber-coax network. The motivation to combine is that it is well known in the art that multipath fading can occur on fiber networks because of impedance mismatches that occurs at connectors, hubs, splitters etc.(See page 1, lines 24-26 of Applicant)

21. Claims 40 is rejected under 35 U.S.C. 103(a) as being unpatentable over Peile(US Patent# 4,821,289) in view of Kurtz (US Patent #6,574,207) further in view of Gollamudi(see PTO-892) further in view of Schilling (US Patent# 6,466,610). Regarding

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Claim 40, Peile, Kurtz, and Gollamudi meet all the limitations of the Claim (please see above paragraphs) except for the use of forward error correcting in a parallel output equalizer.

However, Schilling meets the following limitations:

wherein further processing the parallel outputs comprises forward error correcting the parallel outputs. **(Column 12, line 64 to Column 13, Line 11)**

Therefor it would have been prima facie obvious to one having ordinary skill in the art at the time the invention was made to use forward error correction (FEC) in an equalizer. The motivation to use FEC is that it can reduce bit errors and the bit error rate of the communication system.

22. Claims 41 is rejected under 35 U.S.C. 103(a) as being unpatentable over Peile (US Patent # 4,821,289) in view of Kurtz (US Patent #6,574,207) further in view of Gollamudi (see PTO-892) further in view of Szczepanek (US Patent #5,299,193). Regarding Claim 41, Peile, Kurtz, and Gollamudi meet all the limitations of the Claim (please see above paragraphs) except for the use of detecting errors at packet level.

However, Szczepanek meets the following limitations:

wherein further processing the parallel outputs comprises detecting errors at the packet level.

(Column 11, Lines 15-32)

Therefor it would have been prima facie obvious to one having ordinary skill in the art at the time the invention was made to use packet level error detection. The motivation to combine is that detecting packet level errors can prevent the erroneous decoding of corrupted data.

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23. Claims 43 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Peile(US Patent# 4,821,289) in view of Gollamudi(see PTO-892). Regarding Claim 43, Peile meets the following limitations:

an input adapted to receive signals from a communications channel; **fig 2**

at least one equalizer circuit coupled to the input and operable to generate at least one intermediate signal; **Claim 1, fig 2**

Peile fails to teach the use of a selector circuit for choosing one of the output signals from at least one of the equalizer circuits.

However, Gollamudi discloses the use of such a selector circuit in figure 2 of his adaptive parallel equalization system. Therefor it would have been prima facie obvious to those skilled in the art at the time of the invention to use a switch or selector circuit to chose of the outputs from a bank of parallel equalizers. The motivation to combine is that it is well known in the art that in a parallel configuration of equalizers, memory elements, channels etc. a switch is commonly used to selectively choose one of the plurality of connections or paths based on which equalizer has the best estimate of the channel.

Regarding Claim 44, Peile meets the following limitations:

wherein the at least one equalizer comprises an adaptive equalizer. **(Column 2, lines 29-38)**

24. Claims 45 and 46 is rejected under 35 U.S.C. 103(a) as being unpatentable over Peile(US Patent# 4,821,289) in view of Kurtz (US Patent #6,574,207) further in view of Gollamudi(see PTO-892) further in view of Peile(US Patent# 4,821,288). Regarding Claim 45, Peile, Kurtz, and Gollamudi meet all the limitations of the Claim(please see above paragraphs) except for "loading coefficients for a selected time slot...into a plurality of parallel equalizers."

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However, Peile discloses:

"A significant feature of the invention is that equalization (using a Kalman filter, for example) is performed on the data in each of the time windows A-G of FIG. 4b using separate equalizers for each of the windows. Thus, each time window has its own set of multiplier coefficients (stored in a corresponding one of the tap registers 144a-g and 146a-g) and its own tap update processor (156a-g). Each tap update processor controls the contents of the corresponding pair of tap registers (i.e., the multiplier coefficients) for its own time window independently of all other tap update processors and tap registers. Of course, as illustrated in FIG. 4b, there is some overlap in the data contained in each time window, so that there may be some coincidental correlation between the equalization processes performed in adjacent ones of the time windows A-G of FIG. 4b depending upon codeword length and number of codewords in each interleaved block..."(Column 10, Lines 18-47)

Therefor it would have been prima facie obvious to one having ordinary skill in the art at the time the invention was made to load filter coefficients differently for each selected time window. The motivation to combine is that doing so will create independent uncorrelated equalization between each equalizer in the equalizer bank.

Regarding Claim 46, Peile(US Patent# 4,821,289) meets the following limitations:

wherein equalizing the signal comprises equalizing the signal with a plurality of adaptive equalizers(Column 2, lines 29-38)

25. Claims 47 is rejected under 35 U.S.C. 103(a) as being unpatentable over Peile(US Patent# 4,821,289) in view of Kurtz (US Patent #6,574,207) further in view of Gollamudi(see PTO-892) further in view of Peile(US Patent# 4,821,288) further in view of Schilling (US Patent# 6,466,610). Peile, Kurtz, and Gollamudi met all limitations of Claim 47(see above 103 rejections) except for the use of forward error correcting.

However, Schilling meets the following limitation:

wherein further processing the equalized signals comprises forward error correcting the equalized signals.

Schilling (US Patent# 6,466,610)

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Therefor it would have been prima facie obvious to one having ordinary skill in the art at the time the invention was made to use forward error correction (FEC) in an equalizer. The motivation to use FEC is that it can reduce bit errors and the bit error rate of the communication system.

26. Claims 48 is rejected under 35 U.S.C. 103(a) as being unpatentable over Peile(US Patent# 4,821,289) in view of Kurtz (US Patent #6,574,207) further in view of Gollamudi(see PTO-892) further in view of Peile(US Patent# 4,821,288) further in view of Szczepanek (US Patent #5,299,193). Peile, Kurtz, and Gollamudi met all limitations of Claim 48(see above 103 rejections) except for the use of packet level error detection.

However, Szczepanek meets the following limitation:

wherein further processing the equalized signals includes checking for errors at the packet level.

(Column 11, Lines 15-32)

Therefor it would have been prima facie obvious to one having ordinary skill in the art at the time the invention was made to use packet level error detection. The motivation to combine is that detecting packet level errors can prevent the erroneous decoding of corrupted data.

27. Claims 49 and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Peile(US Patent# 4,821,289) in view of Gollamudi(see PTO-892) further in view of Kurtz (US Patent #6,574,207). Peile and Gollamudi met all limitations of Claim 49 except for the use of the equalization system in a base station.

However, Kurtz meets the following limitations:

at least one base station adapted to provide a connection to a core network; **fig 1**

the base station including a circuit that receives signals from the core network and provides the signals to a plurality of remote users over at least one communication channel; **fig 1**

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the base station further including a receiver that receives time division multiple access signals from a plurality of remote users over at least one communication channel; (**column 6, line 62 to column 7 line 43**)

Therefor it would have been prima facie obvious to one having ordinary skill in the art at the time the invention was made to use a equalization system in a base station. The motivation to combine is that a base station is a common component in a wireless communication system. Also, since wireless system suffer from multipath fading a parallel equalization system, such as the one disclosed by Peile, would be useful in reducing the effects of fading.

Regarding Claim 50, Kurtz meets the following limitations:

wherein the base station comprises a wireless base station. **fig 1**

28. Claims 51 is rejected under 35 U.S.C. 103(a) as being unpatentable over Peile(US Patent# 4,821,289) in view of Kurtz (US Patent #6,574,207) further in view of Gollamudi(see PTO-892) furtherer in view Rakib et al(US Patent# 6,665,308). Peile, Kurtz, and Gollamudi met all limitations of Claim 51 except for the use the base station at hybrid coax head end.

However, Rakib et al meets the following limitations:

wherein the base station comprises a head end of a hybrid fiber-coax network. (**Column 13, Lines 66-67**) and (**Column 1, Lines 28-32**)

Therefor it would have been prima facie obvious to one having ordinary skill in the art at the time the invention was made to use a equalization system in a base station head end of a fiber coax network. The motivation to combine is that a base station is a common component in a head end(or central office) of a wireless network. Since wireless system

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suffer from multipath fading a parallel equalization system, such as the one disclosed by Peile, would be useful in reducing the effects of fading at the central office.

Allowable Subject Matter

29. Claims 7-8, 19-20, 34, 42 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Harry Vartanian whose telephone number is 703.305.8698. The examiner can normally be reached on 9-5:30 Mondays to Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 703.305.4714. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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